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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,774	02/14/2002	Hideo Yamanaka	09792909-5337	9190

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EXAMINER	
TRINH, HOA B	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,774	YAMANAKA ET AL.	
	Examiner	Art Unit	
	Vikki H. Trinh	2814	

-- Th MAILING DATE of this communication app ars on the cover sh t with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,12-26,33-41 and 44-58* is/are rejected.

7)☒ Claim(s) *10,11,27-32,42,43 and 59-61* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims Status

Claims 1-61 are pending in this present application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-9, 12-26, 33-41, 44-58 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. (6,693,044). Yamazaki et al. (6,693,044) discloses a thin semiconductor film formation method for forming a polycrystalline or monocrystalline thin semiconductor film on a substrate, the method comprising:

As to claims 1, 2, 33, 34, a first step of forming a low-crystal-quality (col. 1, lines 46-49) thin semiconductor film 102 on the substrate 100; and a second step of performing focused-light lamp annealing (col. 6, line 62-67) on the low-crystal-quality thin semiconductor film 102 so as to melt or semi-melt (col. 6, line 66) the low-crystal-quality thin semiconductor film or heat the low-crystal-quality thin while maintaining it in a non-melted state and then cool the low-crystal-quality thin semiconductor film thereby enhancing crystallization of the low-crystal-quality thin semiconductor film. See fig. 1E. Note that the term "lamp" has been considered but it is not structurally distinguished over the cited prior art.

As to claims, 3, 12, 35, 44, wherein the first and second steps are performed repeatedly. See col. 7, lines 8-9.

As to claim 4, 36, wherein the focused-light annealing is performed by scanning a focused light ray emitted from a lamp across the substrate such that zone melting recrystallization occurs or by successively scanning a plurality of focused light rays emitted from a plurality of lamps across the substrate such that multiple zone melting recrystallization occurs. See col. 2, lines 1-5.

As to claim 5, it is inherent that scanning is performed by moving the focused light rays emitted from the lamps while maintaining the substrate at a fixed location or by moving the substrate while maintaining the focused light rays at a fixed location. See col. 2, lines 1-5.

As to claims 7, 39, wherein hot air or gas is blown against the front or back side or against botht eh front and the back sides of the substrate during the annealing process. See col. 6, lines 53-58.

As to claims 8, 40, a proper amount of at least one kind of catalytic element is incorporated into the low-crystal-quality thin semiconductor film, and the second step is performed on the low-crystal-quality thin semiconductor film containing the at least one kind of catalytic element. See col. 6, lines 53-54, col. 12, lines 28-40.

As to claims 9, 41, wherein the low-crystal-quality thin semiconductor film is converted into a large-grain polycrystalline form by performing the focused-light annealing. See col. 2, lines 1-5.

As to claims 13, 45, further comprising the step of, before again performing the focused-light annealing, cleaning the surface of the polycrystalline thin semiconductor film or removing a

low-quality oxide film from the surface of the polycrystalline thin semiconductor film by applying, to the polycrystalline thin semiconductor film, a hydrogen-based active species created by means of plasma discharge of hydrogen or a gas containing hydrogen or by means of a catalytic reaction, wherein, after completion of the cleaning step, a low-crystal-quality thin semiconductor film is formed and focused-light annealing is performed. See col. 6, lines 40-55.

As to claims 14, 20, 46, 52, wherein the focused-light annealing is performed in an ambient of reduced-pressure hydrogen, a gas containing reduced-pressure hydrogen, a vacuum, or an atmospheric-pressure nitrogen. See col. 6, lines 63-67.

As to claims 15, 47, in the annealing step the substrate is heated lower than the strain point of the substrate. See col. 7, lines 4-11.

As to claim 16, 48, forming a protective layer 107 (fig. 5B) on the low-crystal-quality thin semiconductor film 103, 104,

As to claims 17, 49, when the focused-light annealing is performed on the low-crystal-quality thin semiconductor film formed on the substrate or when the focused-light annealing is performed on the low- crystal-quality thin semiconductor film coated with a protective insulating film, the substrate is illuminated with the focused light ray emitted from the lamp from above or from below or from both above and below the substrate wherein the substrate is adapted to be transparent (col. 15, lines 11-25) to wavelengths smaller (col. 7, lines 46-48) than 400 nm when the light is applied from below.

As to claims 18, 50, the film coated with protective film is formed into a shape of an island. See figure 5B.

As to claims 19, 51, the illumination of focused light ray is performed in an ambient of atmospheric-pressure nitrogen or in air. See col. 6, line 65, col. 9 ,lines 26-27..

As to claims 21, 53, the annealing is performed while applying a magnetic or electric field. See col. 7, lines 5-12.

As to claims 22, 54, a film of amorphous silicon. See col. 6, line 62.

As to claims 23, 25, 55, 57, forming a thin film transistor, a circuit, an electronic apparatus, liquid display device. See col. 1 ,lines 15-30.

As to claims 24, 56, wherein the focused-light annealing is performed after patterning the low-crystal-quality thin semiconductor film into a form (of one or more islands) corresponding to the channel region, the source region, the drain region, the diode, the resistor, or the electron emission element. See col. 14, lines 6-20.

As to claims 26, 58, wherein when a device such as a semiconductor device, an electro-optical display, or a solid-state imaging device, which includes an internal circuit and a peripheral circuit, is produced, a channel region, a source region, and a drain region of a thin-film insulated-gate field effect transistor of at least one of the internal circuit and the peripheral circuit are formed using the polycrystalline or monocrystalline thin film. See col. 14, lines 6-40.

Allowable Subject Matter

3. Claims 10-11, 27-32, 42-43, 59-61, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record does not disclose or fairly suggest a method of fabricating a semiconductor device having a polycrystalline or monocrystalline thin film disposed on a substrate, the method including the step of forming a layer of a material such as sapphire well lattice-matched with the monocrystalline semiconductor in an area of the substrate where a device is to be formed, step includes forming a low- crystal-quality thin semiconductor film, which may or may not include one or more kinds of catalytic elements, on the crystal layer, and the second step includes performing a focused-light annealing process such that heteroepitaxy growth occurs on the layer acting as a growth seed thereby wherein the first converting the low-crystal-quality thin semiconductor film into the monocrystalline thin semiconductor film.

Response to Arguments

Applicant's arguments filed November 06, 2004, have been fully considered but they are not persuasive.

In the remarks, applicant contends that Yamazaki does not include the limitation in the newly amended claim 1 which states "...focused-light lamp annealing". However, the examiner notes that the term "lamp" is a modifier". This means the feature does not structurally distinguish over the cited prior art. Furthermore, applicant admits that Yamazaki discloses the laser annealing. In laser annealing, the light is focused from a lamp source or the like when it is used to carry out an annealing step. Therefore, Yamazaski meets every limitation of the claims in the present application.

For the foregoing reason, the rejection is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public Pair. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. If you have questions

pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

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HOWARD WEISS
PRIMARY EXAMINER